What is claimed is:

1. A system for transferring data from a peripheral device to a CPU in telecommunications hub operating under UTOPIA protocol, comprising:

a data buffer having data inputs coupled to data outputs of a peripheral device, having data outputs connected to a UTOPIA read data bus, and having a control input for receiving a output enable signal;

address detection logic comprising a register for storing the address of the peripheral device, an input for receiving a read address from the UTOPIA bus, and an output for providing an indication of when the UTOPIA bus address matches the stored address;

a first DFF having a data input coupled to the address detection logic output, a clock input coupled to the UTOPIA bus clock line, and an output indicating the state of the address detection logic output during the preceding clock cycle;

a second DFF having a data input coupled to the UTOPIA bus receive enable line, a clock input coupled to the UTOPIA bus clock line, and an output indicating the state of the UTOPIA bus receive enable line during the preceding clock cycle;

a first AND gate having inputs coupled to the outputs of the first DFF and second DFF, to a read cell available signal output of the peripheral device, and to the UTOPIA bus read enable line and having an output coupled to the data buffer control input.

2. The system of Claim 1, further including:

a second buffer having an input coupled to the peripheral device read start of cell signal output, an output coupled to the UTOPIA bus read start of cell signal line, and having a control input coupled to the AND gate output.

3. The system of Claim 1 further including:

a second AND gate having a first input coupled to the UTOPIA bus receive enable line, a second input, and an output;

an OR gate having inputs coupled to the outputs of the first and second AND gates, and having an output; and

a third DFF having a data input coupled to the output of the OR gate, a clock input coupled to the UTOPIA bus clock line, and having a positive output coupled to the second input of the second AND gate and an output coupled to the data buffer control input.

4. The system of Claim 3, further including:

a second buffer having an input coupled to the peripheral device read start of cell signal output, an output coupled to the UTOPIA bus read start of cell signal line, and having a control input coupled to the third DFF output.

5. A system for transferring a cell available status signal from a peripheral device to a CPU in telecommunications hub operating under UTOPIA protocol, comprising:

a buffer having an input coupled to a cell available output of a peripheral device, having an output connected to a UTOPIA cell available status bus, and having a control input for receiving a output enable signal,

address detection logic comprising a register for storing the address of the peripheral device, an input for receiving an address from the UTOPIA bus, and an output for providing an indication of when the UTOPIA bus address matches the stored address; and

a DFF having a data input coupled to the address detection logic output, a clock input coupled to the UTOPIA bus clock line, and an output coupled to the data buffer control input.

6. A system according to Claim 5 wherein:

the cell available status signal is a read cell available status signal,

the buffer output is coupled to the UTOPIA read cell available signal bus, and

the address detection logic receives the read address signal from the UTOPIA bus.

7. A system according to Claim 5 wherein:

the cell available status signal is a transmit cell available status signal,

the buffer output is coupled to the UTOPIA transmit cell available signal bus, and

the address detection logic receives the transmit address signal from the UTOPIA bus.

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